REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1, 2, 6 and 7 are currently being prosecuted. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

Rejection under 35 U.S.C. § 103

Claims 1, 2, 6 and 7 stand rejected under 35 U.S.C. § 103 as being obvious over the admitted prior art in view of Herman (U.S. Patent No. 4,325,063). This rejection is respectfully traversed.

The Examiner describes the steps of the admitted prior art including receiving a vertical synchronizing signal, receiving a data enable signal, generating a gate clock signal, generating a plurality of gate-on enable signals, generating start vertical signals before the end of the vertical blank period. The Examiner admits that the admitted prior art does not show pausing the output of the CPV and OE signals until the end of the vertical blank period.

The Examiner relies on Herman to teach the pausing of OE' until the end of the vertical blank period. The Examiner feels that it would have been obvious to one of ordinary skill in the art to pause the output of CPV and OE until the end of the vertical blank period as suggested by Herman in the admitted prior art apparatus.

Applicants submit that the present claims are not obvious over this combination of references.

First, it is noted that the admitted prior art does not teach, disclose or suggest that the start vertical signals are generated based on a rising edge or a falling edge of a vertical synchronizing signal. Instead, a control signal of a next frame is generated according to a memory value of horizontal cycle or vertical cycle of the previous frame. If the signals were unstable, a control signal for the next frame will vary. For example, if the start vertical signals are not generated before the end of the vertical blank period, that is, the start vertical signals are not generated until the data enable signal of the next frame is shown, then the display frame of the LCD module will jitter or bounce.

However, the present invention provides a real time process instead of using a memory value of the previous cycle. During each frame, a plurality of gate-on enable signals are simultaneously generated according to the plurality of gate clock cycles after a rising edge or falling edge of the vertical synchronizing signal. Further, after the rising or falling edge, start vertical signals are generated before the end of the vertical blank period and after at least a gate clock cycle during the vertical blank period.

In Herman, after the end of the vertical blanking, the first signal on line CLP causes control unit CTR to terminate the signal

on line OE. That is, the signal on line OE begins being paused after the end of the vertical blanking. However, in the present invention, after the start vertical signals are generated, gate-on enable signals are paused until the end of the vertical blank period. That is, the gate-on enable signals begin being paused before the end of vertical blank period. Herman does not teach that after the start vertical signals are generated that gate-on enable signals are paused until the end of the vertical blank period.

Applicants have amended claims 1 and 6 to indicate that the pausing of the CPV, STV1 and OE signals until the end of the vertical blank period occurs after generating the start vertical signals. This feature is not seen in the admitted prior art and is not disclosed in Herman either. While Herman teaches the pausing of signals until the end of the vertical blank period, it does not teach the relationship as now described regarding the pausing of these three signals after the start vertical signals are generated. Since neither the admitted prior art nor Herman teaches these features, Applicants submit that claims 1 and 6 are not obvious thereover.

Claims 2 and 7 depend from these allowable independent claims and as such are also considered to be allowable. These claims recite other features of the method which makes these claims

additionally allowable. Accordingly, Applicants submit that these claims are also allowable.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejections and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert F. Gnuse (Reg. No. 27,295) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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